REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-29 in the application. In the present response, the Applicant has amended Claims 1, 26, and 19. Support for the amendment can be found, *e.g.*, on lines 18-20 of page 9 and line 10 of page 10 of the substitute specification filed on September 15, 2004. Claims 2-5, 7-8, 17-21, and 23-25 have been amended solely to address the pending indefiniteness rejections. No other claims have been canceled or added. Accordingly, Claims 1-29 are currently pending in the application.

I. Rejection of Claims 2-5, 7-10, and 17-29 under 35 U.S.C. §112

The Examiner has rejected Claims 2-5, 7-10, and 17-29 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. In response, as noted above, the Applicant has amended Claims 2-5, 7-8, 17-21, and 23-25 so that Claims 2-5, 7-10, and 17-29 now comply with the requirements of 35 U.S.C. §112, second paragraph. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §112, second paragraph rejection of Claims 2-5, 7-10, and 17-29 and allow issuance thereof.

II. Rejection of Claim 29 under 35 U.S.C. §102

The Examiner has rejected Claim 29 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,292,845 to Fleck, *et al.* (hereinafter "Fleck"). The Applicant respectfully disagrees in light of the amendment.

Independent Claim 29 (and independent Claims 1 and 26) has been amended, as noted above, to include a limitation that the decode unit receives instruction packets sequentially and detects if each instruction packet is of a first or second class. The detection is carried out using at least one identification bit at a predetermined bit location of the instruction packet. Thus, the invention as presently claimed operates on each packet received sequentially at the decode unit to determine the class (or type) of instruction packet based on at least one identification bit at a predetermined bit location. If the packet is deemed to be of a first class, the control instructions therein are supplied for execution in program order. If, however, the class of packet is determined to be of the second class, including one or more data processing instructions, then instructions in the packet are executed simultaneously. Fleck does not disclose these newly presented claimed elements. Nor does Fleck disclose elements claimed in the original independent Claims as discussed in more detail below.

With respect to previously presented independent Claim 29, the Examiner alleges that Fleck discloses a first and second class of instruction packets. Fleck does not discuss the concept of instruction **packets**. In Fleck, the focus is on individual instructions to determine instruction size and type. Instructions can be taken from memory more than one at a time (*see, e.g.*, the top of column 3 which refers to the instruction stream of 128 bits), but they are not handled in packets at the decode level. Instead, Fleck teaches they are handled as individual instructions in an instruction buffer, where an evaluation unit 7 determines the size of instructions in the instruction stream. The evaluation unit can further determine the type of each instruction. Note, however, that in Fleck, the evaluation unit is focused on individual instructions and does not operate to detect whether instruction **packets** are of a first or second class.

In the invention as presently claimed, the determination of class of packet is carried out by using at least one identification bit at a predetermined bit location in the packet. This makes it very easy for the decode unit to determine what class of packet it has just received. If it has received a packet of the first class, the decode unit automatically supplies the control instructions in execution order. If it receives a packet of the second class, the decode unit operates to supply the instructions in that packet for execution simultaneously.

As such, Fleck does not teach or suggest presently amended independent Claims 1, 26, and 29 and, therefore, does not anticipate presently amended independent Claim 29. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102(b) rejection of Claim 29 and allow issuance thereof.

III. Rejection of Claims 1-3, 6-10, 12 14, 17, 19, and 21-28 under 35 U.S.C. §103

The Examiner has rejected Claims 1-3, 6-10, 12 14, 17, 19, and 21-28 under 35 U.S.C. §103(a) as being unpatentable over Fleck in view of U.S. Patent Application Publication 2004/0054876 by Grisenthwaite, *et al.* (hereinafter "Grisenthwaite"). The Applicant respectfully disagrees.

As established above, the cited portions of Fleck do not teach or suggest presently amended independent Claims 1 and 26. With respect to previously presented independent Claim 1, the Examiner suggests that Fleck discloses "wherein the decode is operable to receive an instruction **packet** and to detect if the instruction **packet**..." **(Emphasis added.)** As noted above, Fleck does not look at packets in the decode unit, but looks at individual instructions to ascertain their size and/or type. The portion of Fleck referred to by the Examiner at lines 47 to 52 of column 3 merely

states that if two instructions of the same kind follow each other, only one single instruction is sent to each of the pipeline structures and a no-op instruction is sent to another of the pipeline structures. There is no disclosure of detecting an instruction packet class and handling the instructions in the packet in accordance with the detected class as presently claimed.

Similarly, with respect to independent method Claim 26, Fleck does not disclose step (b) "decoding each instruction **packet** in turn by determining if the instruction **packet** defines..." **(Emphasis added.)** Therefore, Fleck does not disclose the steps of following this step of either supplying control instructions to the first class for execution in program order, or the plurality of instructions in a second class of packet for execution simultaneously.

For at least the reasons given above, the cited portions of Fleck do not teach or suggest each and every limitation of presently amended independent Claims 1 and 26. Grisenthwaite has not been cited to cure the above-noted deficiencies of Fleck but to teach a processor with two pipelines that can execute the same types of instructions. As such, the cited portions of the cited combination of Fleck and Grisenthwaite, as applied by the Examiner, do not provide a *prima facie* case of obviousness for presently amended independent Claims 1 and 26 and Claims that depend thereon. Accordingly, the Applicant respectfully request the Examiner to withdraw the §103(a) rejection of Claims 1-3, 6-10, 12 14, 17, 19, and 21-28 and allow issuance thereof.

IV. Rejection of Claims 4-5, 11, 13, 15-16, 18, and 20 under 35 U.S.C. §103

The Examiner has rejected Claims 4-5, 11, 13, 15-16, 18, and 20 under 35 U.S.C. §103(a) as being unpatentable over Fleck in view of Grisenthwaite and further in view of: U.S. Patent No. 6,880,150 to Takayama, *et al.* (hereinafter "Takayama") for Claims 4-5 and 11; U.S. Patent No.

5,956,518 to DeHon, *et al.* (hereinafter "DeHon") for Claims 13 and 15; U.S. Patent No. 7,234,042 to Wilson (hereinafter "Wilson") for Claim 16; U.S. Patent No. 6,725,357 to Cousin (hereinafter "Cousin") for Claim 18; and a paper entitled "Variable Length Instruction Compression for Area Minimization," by Simonen, *et al.* (hereinafter "Simonen") for Claim 20. The Applicant respectfully disagrees.

As established above, the cited portions of the cited combination of Fleck and Grisenthwaite, as applied by the Examiner, do not provide a *prima facie* case of obviousness for presently amended independent Claims 1 and 26. Takayama, DeHon, Wilson, Cousin, and Simonen have not been cited to correct the above-noted deficiencies of the cited combination of Fleck and Grisenthwaite but to teach the subject matter of the above-mentioned dependent Claims. As such, the cited portions of Fleck and Grisenthwaite in view of Takayama, DeHon, Wilson, Cousin, or Simonen do not provide a *prima facie* case of obviousness for presently amended independent Claims 1 and 26 and Claims that depend thereon. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 4-5, 11, 13, 15-16, 18, and 20 and allow issuance thereof.

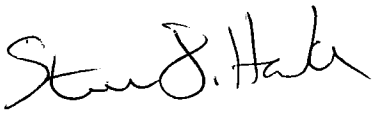
V. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-29.

The Applicant requests the Examiner to telephone the undersigned agent of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

HITT GAINES, PC



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